Rapid advancements in heterogeneous architectures have placed incremental challenges on programming productivity, portability, and performance on such systems. From high-end servers to mobile devices, from specialized accelerators to embedded SoCs, from single node multicore/manycore to distributed clusters in cloud, be it NVIDIA, ARM, Intel, AMD or Cray, there are a many complex low-level details needed to be managed and abstracted from the programmers.

The PMHS workshop aims to bring together researchers and industrial practitioners both from computer architecture scientists and the software engineering community to present the latest ideas and findings in all aspects of heterogeneous system programming models, language design or extension, compilers design or optimization, runtime systems, and programming tools. The objective is to brainstorm ways to make programming heterogeneous systems less challenging and more interesting, and promote the synergies between hardware design and software design.

Topics of interest to the PHMS workshop include but are not limited to:

- Programming environments for accelerators, embedded/SoC systems, and multicore/manycore processors, such as GPUs, FPGAs, Cells, MICs, etc.
- Programming environments for large-scale parallel systems, clusters of multicore/manycore, distributed big-data systems, and SDN.
- Compiler optimizations and tuning heterogeneous systems
  - Parallelization and loop transformations/fusion
  - Locality/affinity optimizations
  - SIMDization/Vectorization
  - Reducing synchronization & scheduling overheads
  - Tiling and offloading
- Innovative runtime systems for multicore processors, heterogeneous systems, and accelerators.
Scalable tools for performance analysis, modeling, monitoring, and debugging.
• Programming language/models: thread and task based models, data parallel models, stream programming models, shared/distributed memory models, PGAS, etc.
• Hardware-software co-design, OS and architectural support for parallel programming.
• Improvements for existing parallel languages and run-time environments such as MPI, OpenMP, Cilk, OpenACC, OpenCL, CUDA, ArrayFire, FastFlow, OpenSHMEM, UPC, Co-Array Fortran (CAF), Titanium, GASPI, X10, and Chapel, etc.

Manuscript Submission & Proceedings

Papers reporting original and unpublished research results are solicited. All submissions will be handled electronically through EasyChair (https://easychair.org/conferences/?conf=pmhs2015). Submissions will be judged by at least 3 reviews on originality, technical strength, quality of presentation, and relevance to the workshop scope. The length of the camera-ready manuscripts will be limited to 4 pages (6 pages with the over length charge) in standard IEEE CS proceedings paper format (two-column).

All accepted papers will be included in the HPCC-2015 Workshop Proceeding published by IEEE Computer Society (indexed by EI). Authors of selected papers in PMHS 2015 will be invited to extend their papers for submission to special issues in prestigious SCI & EI indexed Journals. Authors of accepted papers, or at least one of them, are required to register and present their work at the conference, otherwise their papers will not be published.

Important Dates:

April 30, 2015: Due date for full workshop papers submission
June 15, 2015: Notification of paper acceptance to authors
July 15, 2015: Camera-ready of accepted papers
August 24-26: Workshop in conjunction with HPCC 2015

Workshop Organization

Co-chairs:

• Lin Ma Huawei America Research Center, USA
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Program Committee (to be extended):

• Peng Li Amazon, USA
• Robert Utterback Washington University in Saint Louis, USA
• Chengjie Wu Yahoo, USA
• Xingjing Lu ICT, Chinese Academy of Sciences, China
• Wenlei Bao Ohio State University, USA
• Fenglong Song  Huawei, China
• Lingjun Fan  ICT, Chinese Academy of Sciences, China
• Jing Li  Washington University in Saint Louis, USA
• Jiefan Qiu  Zhejiang University, China
• Shigang Li  IGT, Chinese Academy of Sciences, China